MARK UP VERSION OF AMENDMENTS

C.

Referring now to Fig. [8] 20, partially reduced metal silicate layer 50 is converted to a silicate layer 52 by oxidation. Control of oxidation is critical during this step, as under-oxidation will result in decreased resistivity and over-oxidation may result in decreased capacitance for layer 52 (due to oxidation of the underlying silicon). Post-anneals in O_2 at about 400-550° for up to about 30 minutes generally increase capacitance while maintaining low leakage current. Anneals at higher temperatures or longer times tend to degrade capacitance.

REMARKS

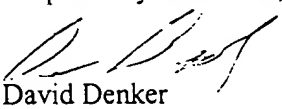
Claims 1 - 30, 36 - 40, and 46 - 80 are now pending. This amendment cleans up minor errors in the specification and adds Fig. 21. Applicants respectfully request reconsideration of the restriction requirements.

1. Applicants have added Fig. 21 as requested. One instance of specific support can be found in the text of pages 14 - 18 describing Embodiment 1, the transistor background on pages 1 and 2, Fig. 1, and Fig. 9.

2. Applicants have added text to support Fig. 21, as well as fix several inadvertent errors in the description of the original figures.

3. Applicants believe that the application is in condition for allowance. If Examiner has any further comments or suggestions, Applicants respectfully request that Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

Respectfully submitted,



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